Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (NEW) EXAMINATION – SUMMER 2022

Subject Code:2131004 Date:18-07-2022

Subject Name:Digital Electronics

Time:02:30 PM TO 05:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	1.Convert the binary number (1101110.0110) to Hexadecimal 2. Find 2's Complement Representation of $(-45)_{10}$. 3. Convert $(FFFF)_{16}$ = (_____)$_8$	**03**
	(b)	Implement the function F(a,b,c) = Σ (0,6) with 1.Only NAND Gates. 2. Only NOR Gates	**04**
	(c)	With a neat block diagram explain the function of encoder. Explain priority encoder?	**07**
Q.2	**(a)**	Simply Boolean Function: F=(B+BC)(B+B'C)(B+D)	**03**
	(b)	Discuss Clocked R-S Flip-flop with Logic diagram, Symbol, Characteristic table and Characteristic equation	**04**
	(c)	Design BCD adder using binary parallel adder.	**07**
		OR	
	(c)	Generate AND, OR, NOT, EXOR and EX-NOR gate using NAND as a universal gate.	**07**
Q.3	**(a)**	What is "Lock out" condition in counter? How to avoid it.	**03**
	(b)	Implement Full Adder Circuit with the help of Decoder and logic gates.	**04**
	(c)	Explain working of master-slave JK flip-flop with necessary logic diagram, state equation and state diagram	**07**
		OR	
Q.3	**(a)**	Implement T flip flop using JK flip flop.	**03**
	(b)	Implement the Boolean function F(X,Y,Z)= ∑(0,2,3,4) using suitable multiplexer.	**04**
	(c)	Reduce the expression f=ΠM(0,1,2,3,4,7) using K Map and draw the circuit with NOR gates only.	**07**
Q.4	**(a)**	Draw logic circuit for 2-Bit Magnitude Comparator.	**03**
	(b)	Write a short note on ring counter.	**04**
	(c)	Design a counter using T FF for following binary sequence 0-1-3-4-6-0.	**07**
		OR	
Q.4	**(a)**	Define State Table and State Diagram.	**03**
	(b)	Discuss advantages and drawbacks of TTL logic family	**04**
	(c)	Design 4 bit asynchronous up counter.	**07**
Q.5	**(a)**	Compare asynchronous and synchronous state machines.	**03**

	(b)	Write short note on Programmable Logic Arrays.	**04**
	(c)	With suitable design example discuss the basic design principles of Asynchronous State Machines design	**07**
		OR	
Q.5	**(a)**	Explain following terms w.r.t Digital Logic Family. 1. Fan-in 2. Noise Margin 3. Power Dissipation	**03**
	(b)	Explain 4-Bit serial in serial out shift register	**04**
	(c)	Compare ROM, PLA and PAL.	**07**

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